Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for fabricating a semiconductor structure, comprising:

depositing a polysilicon layer on the semiconductor substrate;

removing a portion of the polysilicon layer to form a high region and a low region;

forming a silicide layer over the semiconductor substrate; ~~and~~

selecting chemical mechanical polishing parameters to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate, where the first rate is higher than the second rate; and

removing a portion of the silicide layer by chemical mechanical polishing at the first rate.

2. (Currently Amended) The method of claim 1, ~~further comprising:~~

~~forming a high region and a low region on the semiconductor substrate,~~

wherein the high region and the low region are formed before the silicide layer is formed and the portion of the silicide layer removed by chemical mechanical polishing is removed from the high region.

3. (Canceled)

4. (Canceled)

5. (Original) The method of claim 1, further comprising:

forming a dielectric layer over the silicide layer; and

removing a portion of the dielectric layer to expose the portion of the silicide layer before removing the portion of the silicide layer.

6. (Original) The method of claim 5, wherein the dielectric layer comprises silicon dioxide.

7. (Original) The method of claim 5, wherein the dielectric layer comprises silicon nitride.

8. (Original) The method of claim 5, wherein the portion of the dielectric layer is removed by chemical mechanical polishing.

9. (Original) The method of claim 5, further comprising forming a top layer after forming the dielectric layer and removing a portion of the top layer before removing the portion of the dielectric layer.

10. (Original) The method of claim 9, wherein the top layer comprises a titanium nitride layer.

11. (Original) The method of claim 10, wherein the portion of the titanium nitride layer is removed by chemical mechanical polishing.

12. (Original) The method of claim 11, wherein the portion of the titanium nitride layer is removed with a first slurry and the portion of the dielectric layer is removed with a second slurry.

13. (Currently Amended) The method of claim 12, wherein a polishing rate of the titanium nitride layer ~~polishing rate~~ with the first slurry is greater than a polishing rate of the dielectric layer with the ~~first~~ second slurry.

14. (Original) The method of claim 12, wherein a polishing rate of the titanium nitride layer with the second slurry is less than a polishing rate of the dielectric layer with the second slurry.

15. (Currently Amended) A method for fabricating a semiconductor structure, comprising:

forming a polysilicon feature on a semiconductor substrate having an intermediate gate dielectric layer;

depositing a first metal layer over the polysilicon feature;

reacting the first metal layer with the polysilicon feature to form a metal silicide;

depositing a dielectric layer over the metal silicide and the semiconductor substrate;

removing a portion of the dielectric layer over the metal silicide to expose a portion of the metal silicide; ~~and~~

removing the portion of the metal silicide by chemical mechanical polishing;

removing the polysilicon feature to create an opening in the gate dielectric layer;

removing the gate dielectric layer; and

oxidizing the semiconductor substrate to form a new gate dielectric layer.

16. (Original) The method of claim 15, wherein the portion of the dielectric layer is removed by chemical mechanical polishing.

17. (Currently Amended) The method of claim 16, wherein the dielectric layer ~~has~~ is removed at a first polishing rate, the metal silicide ~~has~~ is removed at a second polishing rate, and the first polishing rate is different from the second polishing rate.

18. (Canceled)

19. (Currently Amended) The method of claim 15 ~~18~~, further comprising:

filling the opening in the gate dielectric layer with a ~~second~~ metal.

20. (Currently Amended) A method for fabricating a semiconductor structure, comprising:

depositing a material over a semiconductor substrate,

patterning the material to define a topography having a high region and a low region;

forming a metal silicide in the high region of the topography and in the low region of the topography; ~~and~~

selecting chemical mechanical polishing parameters to remove the metal silicide at a first rate, and to remove the material at a second rate, where the first rate is higher than the second rate; and

removing the metal silicide from the high region of the topography by chemical mechanical polishing at the first rate.

21. (Original) The method of claim 20, wherein the high region comprises a polysilicon feature.

22. (Currently Amended) The method of claim 21 ~~20~~, wherein the chemical mechanical polishing of the metal silicide is faster than the chemical mechanical polishing of the polysilicon feature ~~material defining the topography~~.